CLAIMS

What is claimed is:

1. A DSP (Digital Signal Processing) architecture with a wide memory bandwidth, the DSP architecture comprising:

a first communication port;

first, second, and third memory devices, which are connected with the first communication port and are arranged in a first row direction of the DSP architecture;

a fourth memory device, a calculation element, and a fifth memory device, which are arranged in a second row direction below the first row direction of the DSP architecture; and

sixth, seventh, and eighth memory devices, which are connected with the first communication port and arranged in a third row direction of the DSP architecture,

wherein the calculation element is connected with the first through the eight memory devices.

2. The DSP architecture of claim 1, further comprising a second communication port, which is connected with the first, the fourth, and the sixth memory devices arranged in a first column direction of the DSP architecture, and with the third, the fifth, and the eighth memory devices arranged in a third column direction of the DSP architecture.

3. The DSP architecture of claim 2, wherein the second and seventh memory devices are connected to the second communication port through the calculation elecment and arranged in a second column direction of the DSP architecture.

4. The DSP architecture of claim 3, wherein the second column direction is disposed between the first and the third column directions.

5. The DSP architecture of claim 4, wherein the second row direction is disposed between the first and the third row directions.

6. The DSP architecture of claim 1, wherein the calculation element and the first through the eighth memory devices form one arrangement unit, wherein the calculation element is disposed in the center of the arrangement unit, the first through the eighth memory devices are connected to the calculation element, and the arrangement unit is arranged in row directions

and column directions of the DSP architecture.

7. A memory mapping method to process an image, which is used in a DSP architecture, the method comprising:

storing data received through a first communication port in first and second memory devices arranged in a first row direction of the DSP architecture;

storing the data received through the first communication port in a third memory device arranged in a second row direction of the DSP architecture, wherein the data is stored in the third memory device, through a first calculation element that is connected with the first and the second memory devices and neighboring with the third memory device in the second row direction; and

processing the data stored in the first through the third memory devices using the first calculation element.

8. The memory mapping method of claim 7, comprising:

storing the data processed by the first calculation element in a fourth memory device neighboring with the second memory device in the first row direction of the DSP architecture, and in a fifth memory device neighboring with the first calculation element in the second row direction of the DSP architecture; and

processing the data stored in the fourth and the fifth memory devices using a second calculation element neighboring with the fifth memory device in the second row direction of the DSP architecture.

9. A memory mapping method to process an image, which is used in a DSP architecture, the memory comprising:

storing data received through a first communication port in first and second memory devices arranged in a first row direction of the DSP architecture;

storing the data received through the first communication port in fourth and fifth memory devices arranged in a third row direction of the DSP architecture;

storing the data received through the first communication port in a third memory device arranged in a second row direction of the DSP architecture, wherein the data is stored in the third memory device, through a first calculation element connected with the first and the second memory devices and neighboring with a third memory device in the second row direction;

storing the data received through the first communication port in a sixth memory device

arranged in a fourth row direction of the DSP architecture, wherein the data is stored in the sixth memory device, through a second calculation element connected with the fourth and the fifth memory devices and neighboring with the sixth memory device;

processing the data stored in the first through the third memory devices using the first calculation element; and

processing the data stored in the fourth through the sixth memory devices using the second calculation element.

10. The memory mapping method of claim 9, further comprising:

storing the data calculated by the first calculation element in a seventh memory device neighboring with the second memory deice in the first row direction of the DSP architecture, and in an eighth memory device neighboring with the first calculation element in the second row direction of the DSP architecture;

processing the data stored in the seventh and the eighth memory devices using a third calculation element neighboring with the eighth memory device in the second row direction of the DSP architecture;

storing the data calculated by the second calculation element in a ninth memory device neighbouring with the fifth memory device in the third row direction of the DSP architecture, and in a tenth memory device neighboring with the second calculation element in the fourth row direction of the DSP architecture; and

processing the data stored in the ninth and the tenth memory devices using a fourth calculation element neighboring with the tenth memory device in the fourth row direction of the DSP architecture.

11. A memory mapping method to process an image, which is used in a DSP architecture, the method comprising:

storing data received through a first communication port in first, second, and third memory devices arranged in a first row direction of the DSP architecture, or in sixth, seventh, and eighth memory devices arranged in a third row direction of the DSP architecture;

storing data received through a second communication port in the first and the sixth memory devices and a fourth memory device that are arranged in a first column direction of the DSP architecture, or in the third and the eighth memory devices and a fifth memory device that are arranged in a third column direction of the DSP architecture; and

processing the data stored in the first through the eighth memory devices, using a

calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture.

12. A DSP (Digital Signal Processing) architecture with a wide memory bandwidth, the DSP architecture comprising:

a first communication port;

at least three memory devices connected with the first communication port and arranged in a first row direction of the DSP architecture;

at least two memory devices arranged in a second row direction below the first row direction of the DSP architecture;

at least three memory devices connected with the first communication port and arranged in a third row direction of the DSP architecture, and

a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture.

13. The DSP architecture of claim 12, further comprising a second communication port connected with at least two memory devices in each of the first, second and third rows of the DSP architecture.

14. A DSP (Digital Signal Processing) architecture, comprising:

a first communication port;

a second communication port; and

a first arrangement unit connected to the first communication port and the second communication port,

wherein the first arrangement unit comprises first through eight memories and a calculation element which are arranged in a matrix structure having three columns and three rows, the second and seventh memories are connected to the second communication port through the calculation element, and the fourth and fifth memories are connected to the first communication port through the calculation element.

15. The DSP architecture of claim 14, further comprising:

a third communication port; and

a second arrangement unit connected to the third communication port and to the first

and second communication parts through the sixth and the eight memories of the arrangement unit, wherein the second arrangement comprises eight memories and a second calculation element which are arranged in a matrix structure having three columns and three rows.

16. The DSP architecture of claim 15, further comprising:

a third calculation element and two memories which are disposed between the first and second arrangement units, wherein the two memories are connected to the memories of the first and second arrangement units through the third calculation element.